IN THE CLAIMS

Please amend the claims as shown below. Please cancel Claims 1-5, 10-13, and 17 without prejudice. Claims 6, 8-9, 14, 16, 18, and 20 are amended herein. New Claims 21-30 follow amended Claim 20; no new matter is added. This listing of claims will replace all prior versions and listings of claims in the Application.

1-5. (Cancelled)

6. (Currently Amended) ~~The semiconductor structure as recited in Claim 5 wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.~~ A semiconductor structure comprising:

a pad area;

an electrostatic discharge protective device disposed below said pad area, said electrostatic discharge protective device comprising a transistor and a resistance, wherein said pad area comprises:

a substrate;

a first layer of metal disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal; and

a second layer of metal disposed above said first layer of metal;

a layer of dielectric disposed between said first metal layer and said second metal layer; and

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias and wherein said resistance comprises a portion of said plurality of

individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

7. (Original) The semiconductor structure as recited in Claim 6 wherein a resistive value of said resistance is fixed during a process for fabricating said semiconductor structure.

8. (Currently Amended) The semiconductor structure as recited in Claim 7 wherein said resistive value of said resistance is fixed with ~~by a method selected from the group consisting essentially of:~~ setting a particular number for said portion of said plurality of individual vias in parallel[[;]]

~~forming said individual vias comprising said portion of said plurality of individual vias with a particular cross-sectional area; and~~

~~forming said individual vias comprising said portion of said plurality of individual vias with a particular length~~.

9. (Currently Amended) The semiconductor structure as recited in Claim 6 [[3]] further comprising a subsequent layer of metal between said first and said second metal layers.

10-13. (Cancelled)

14. (Currently Amended) ~~The pad area apparatus as recited in Claim 13 wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.~~ A pad area apparatus for a semiconductor structure comprising:

a substrate;

a first layer of metal disposed above said substrate;

a second layer of metal disposed over said first layer of metal;

an electrostatic discharge protective device wherein said electrostatic discharge protective device is disposed within said substrate and wherein said electrostatic discharge protective device comprises a transistor and a resistance;

a layer of dielectric disposed between said first metal layer and said second metal layer; and

a via disposed within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias, and wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

15. (Original) The pad area apparatus as recited in Claim 14 wherein a resistive value of said resistance is fixed during a process for fabricating said semiconductor structure.

16. (Currently Amended) The pad area apparatus as recited in Claim 15 wherein said resistive value of said resistance is fixed with ~~by a method selected from the group consisting essentially of:~~

setting a particular number for said portion of said plurality of individual vias in parallel[[;]]

~~forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area; and~~

~~forming said individual vias comprising said portion of said plurality of individual vias with a particular length~~.

17. (Cancelled)

18. (Currently Amended) An electrostatic discharge protective device for a semiconductor structure comprising:

a resistance; and

a transistor disposed within a substrate below a pad area of said semiconductor structure, ~~The electrostatic discharge protective device as recited in Claim 17~~ wherein said resistance comprises a plurality of vias of said semiconductor structure, wherein said vias are arranged electrically in parallel, one to another.

19. (Original) The electrostatic discharge protective device as recited in Claim 18 wherein a resistive value of said resistance is fixed during a process for fabricating said semiconductor structure.

20. (Currently Amended) The electrostatic discharge protective device as recited in Claim 19 wherein said resistive value of said resistance is fixed with ~~by a method selected from the group consisting essentially of:~~

setting a particular number for said portion of said plurality of individual vias in parallel[[;]]

~~forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area; and~~

~~forming said individual vias comprising said portion of said plurality of individual vias with a particular length~~.

21. (New) The electrostatic discharge protective device as recited in Claim 19 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

22. (New) The electrostatic discharge protective device as recited in Claim 19 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

23. (New) The pad area apparatus as recited in Claim 15 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

24. (New) The pad area apparatus as recited in Claim 15 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

25. (New) The semiconductor structure as recited in Claim 7 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

26. (New) The semiconductor structure as recited in Claim 7 wherein said resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.

27. (New) A method of fabricating an semiconductor structure, comprising:

disposing a pad area upon a substrate;

disposing an electrostatic discharge protective device below said pad area, said electrostatic discharge protective device comprising a transistor and a resistance, wherein said pad area comprises:

a first layer of metal disposed above said substrate wherein said electrostatic discharge protective device is disposed below said first layer of metal; and

a second layer of metal disposed above said first layer of metal;

disposing a layer of dielectric between said first metal layer and said second metal layer; and

disposing a via within said dielectric layer wherein said via electrically couples said first and said second metal layer, wherein said via comprises a plurality of individual vias and wherein said resistance comprises a portion of said plurality of individual vias, wherein said individual vias comprising said portion are arranged electrically in parallel one to another.

28. (New) The method as recited in Claim 27 wherein a resistive value of said resistance is fixed with setting a particular number for said portion of said plurality of individual vias in parallel.

29. (New) The method as recited in Claim 27 wherein a resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular cross sectional area.

30. (New) The method as recited in Claim 27 wherein a resistive value of said resistance is fixed with forming said individual vias comprising said portion of said plurality of individual vias with a particular length.